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Docket No.: NL00 0667

TO: Examiner: Brett J. BUEHL

Art Unit: 2183

Fax Number: (571) 273-8300

FROM: Michael J. Ure, Reg. No. 33,089

Telephone: (408) 474 - 9077

TRANSMISSION INCLUDES: 37 Pages (including cover sheet)

Appeal Brief (in triplicate) – 12 pages

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on 9/20, 2005 by _____
Daniel L. Michalek

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
Intellectual Property & Standards
1109 McKay Drive M/S-41SJ
San Jose, California 95131
Telephon Number: (408) 474-9066
Fax Number: (408) 474-9080

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	**Pessolano**
Application No.	:	**10/020,019**
Filed	:	**December 7, 2001**
For	:	**DIGITAL SIGNAL PROCESSING APPARATUS**

APPEAL BRIEF

On Appeal from Group Art Unit 2183

Date: September 20, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

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Daniel L. Michalek
(Name)

20-SEP-2005
(Signature and Date)

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Claims 1-3, 5-11, 13 and 14 are pending. All of these claims stand finally rejected, and form the subject matter of the present appeal.

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V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a data processing arrangement having multiple instruction execution units in which control of at least some of the execution units is a combination of global control and local control. Such a processing arrangement is illustrated in Fig. 5 of the specification and described, *inter alia*, in the paragraph

bridging pages 8 and 9 of the specification. Fig. 5 may be contrasted with the prior art arrangement of Fig. 2b. Compared with conventional arrangements, the invention results in increased performance because it is easier to keep the functional units busy. Furthermore, fewer program memory accesses are required, resulting in lower power and lower memory bandwidth requirements.

Indpendent claim 1 relates to a digital signal processing apparatus for executing a plurality of operations, including a plurality of functional units wherein each functional unit is adapted to execute operations, and control means for controlling said functional units. The control means comprises a fetch unit, a decode unit, and a plurality of control units responsive to said decode unit. At least one control unit is operatively associated with a respective functional unit for controlling its function, including controlling a number of repetitions of execution of its function, and each functional unit is adapted to execute operations in an autonomous manner under control of the control unit associated therewith.

Independent claim 10 relates to a method for processing digital signals in a digital signal processing apparatus having a plurality of functional units wherein each functional unit is adapted to execute operations. The functional units are controlled by control means including a single fetch unit, a single decode unit and a plurality of control units. At least one control unit is operatively associated with a respective unit so that each functional unit is able to execute operations in an autonomous manner under control of the control unit associated therewith, the control unit controlling a number of repetitions of execution of its associated functional unit.

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. claims 1-3, 5-11, 13 and 14 are anticipated by White.

Applicant acquiesces in the rejections of claims 5 and 14 under USC 112, second paragraph. No review of these rejections is sought.

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I. Rejection of Claims 1-3, 5-11, 13 and 14 as anticipated by White

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Details of a reservation station are shown in Fig. 5A of White and described in columns 21 and 22. Note column 22, lines 9-23:

> When all information necessary to execute an ROP instruction has been assembled in the functional unit, the ROP instruction is then issued to execution unit 345 for execution. More particularly, the A operand and the B operand are provided to execution unit 345 by the reservation station. The opcode and destination tag for that instruction are provided to execution unit 345 by the tag and opcode location 380. The execution unit executes the instruction and generates a result. The execution unit then arbitrates for access to the result bus by sending a result request signal to an arbitrator (not shown). When the execution unit 345 is granted access to the result bus, a result grant signal is received by execution unit 345 from the arbitrator. Execution unit 345 then places the result on the designated result bus.

It may be seen therefore than in White, the "control unit" (reservations stations) *do not* control of a number of repetitions of execution of a functional unit as claimed.

With respect to claim 3, which was previously presented, the rejection describes "FIFO...register means adapted for supporting data-flow communication among said

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Applicant respectfully disagrees. There is no indication in White that the Reorder Buffer of White is a FIFO register. Typically, the Reorder Buffer of White would not be expected to be realized using a FIFO register.

Accordingly, the White cannot be said to anticipate the inventions recited in claims 1 and 10.

With regard to dependent claims 2, 3, and 5-9, and dependent claims 11, 13 and 14, these claims depend from independent claims 1 and 10, respectively, which have been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claims.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: September 20, 2005

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

IX. APPENDIX: THE CLAIMS ON APPEAL

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2. An apparatus according to claim 1, characterized by FIFO (first-in/fist-out) register means adapted for supporting data-flow communication among said functional units.

3. A digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, and control means for controlling said functional units in coordination with one another in response to a single fetch unit and a single decode unit, characterized by FIFO (first-in/fist-out) register means adapted for supporting data-flow communication among said functional units.

5. Apparatus according to any one of claims 2, characterized in that said FIFO register means comprises a plurality of FIFO registers.

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7. An apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage comprises a functional unit.

8. An apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, where-in said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit .

9. An apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units.

10. A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, characterized in that said functional units are controlled by control means including a single fetch unit, a single decode unit and a plurality of control units wherein at least one control unit is operatively associated with a respective unit so that

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11. An apparatus according to claim 9, characterized in that data-flow communication among said functional units is supported by FIFO (first-in/first-out) register means .

13. An apparatus according to claim 11, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by a functional unit .

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X. APPENDIX: RELATED PROCEEDINGS

NONE

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Date: September 20, 2005

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